TRANSISTOR LEVEL COMPARATOR DESIGN

STUDENTS / UNIVERSITIES

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Introduction

Analog to digital converters are widely used in digital circuits such as smart-phones, in order to process natural, analog signals. As sampling rate of analog signal increases, digital signal becomes more accurate. That's why it is aimed to make a fast and low power ADC's.

Comparator is an essential part of ADC circuits, which compares two voltage inputs at each clock pulse and gives a single bit decision, logic 1 or 0. Thus, it directly affects the speed and power consumption of ADC circuits. In this project, it is aimed to design a comparator in transistor level with high speed to power ratio, using 130 nm CMOS technology.

Mobile Phone Architecture

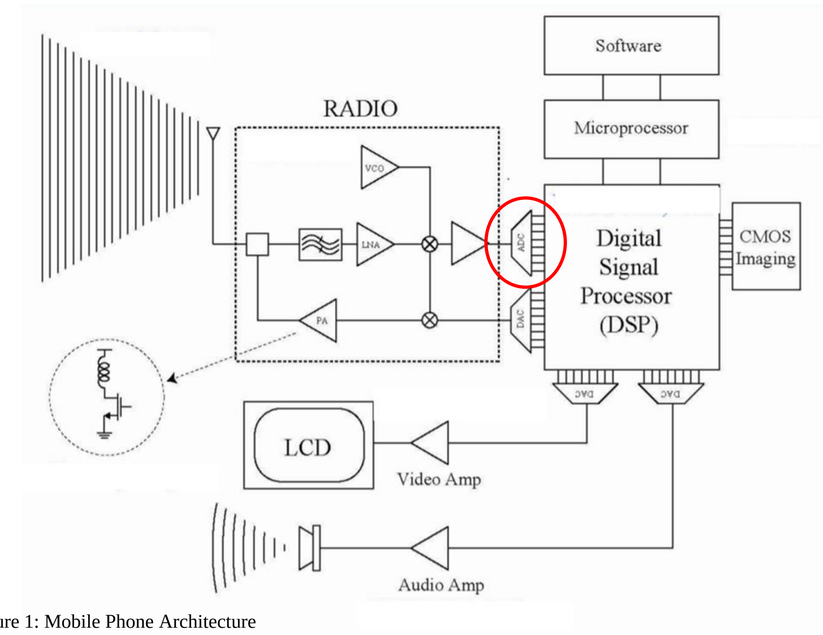

Figure 1: Mobile Phone Architecture

- While having a call, or connecting to internet, radio stage which is an analog circuit, receives analog signal from antenna.
- It is not possible to process analog signal in digital signal processor. It has to be converted into a digital signal by taking samples in ADC.
- To send a data using antenna, visualize a frame in LCD screen, or play a sound using speaker, digital data from DSP has to be converted back to analog signal using DAC.
- In order to hear the received signal clearly while having a phone call, before sending the signal to speakers, DAC should be able to reconstruct digital signal accurately.
- For this purpose, ADC should be able to work fast and take as many samples as possible from analog signal during conversion to digital.

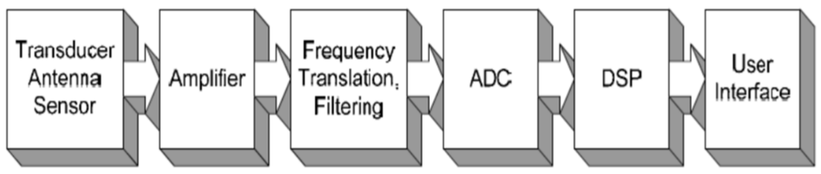

Figure 2: Antenna to User Interface Progress

Analog vs Digital Signals

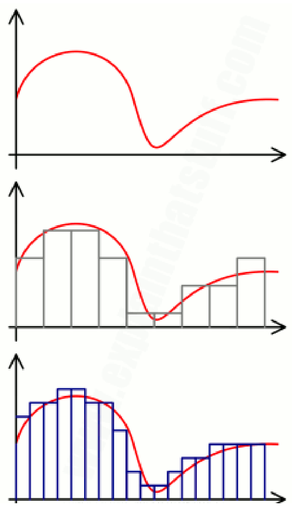

Figure 3: Analog and Digital Signals

- Analog signals are continuous time data sequences, that are abundant in nature .
- Converting to a digital signal means taking samples from the analog signal with specified sampling frequency.
- As the sampling frequency increases, resultant digital signal looks similar to analog signal.
- To increase the sampling rate, ADC should be able to work at high speeds.

Acknowledgements

- A New Ultra Low Power High Speed Dynamic Comparator, Khalafi, Ali, Ahmad Rabiei, Arman Najafizadeh, 2015
- HIGH-SPEED AND LOW-POWER DYNAMIC LATCH COMPARATOR, Moni, Jackuline, P. Jisha
- Allen, P. E., & Holberg, D. R. (2016). *CMOS analog circuit design*. New Delhi, India: Oxford University Press.

Analog to Digital Converter

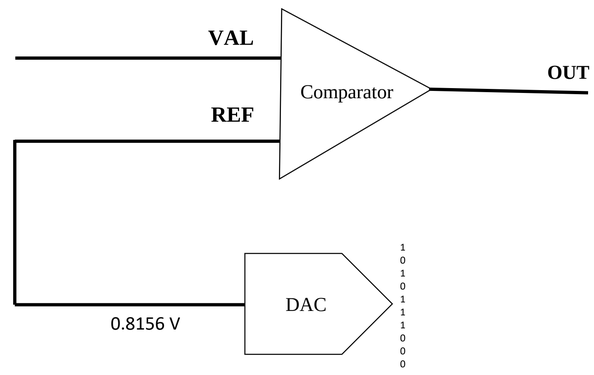

Figure 4: Analog to Digital Converter Outline

- Converts analog values into digital binary values.
- At each iteration, comparator compares reference (REF) voltage coming from DAC and analog value (VAL).
- If value is higher than or equal to reference, it returns logic 1, else 0.
- At 10 iterations, it can convert an analog voltage value to a number between 0 and 1023.

Designed Comparator

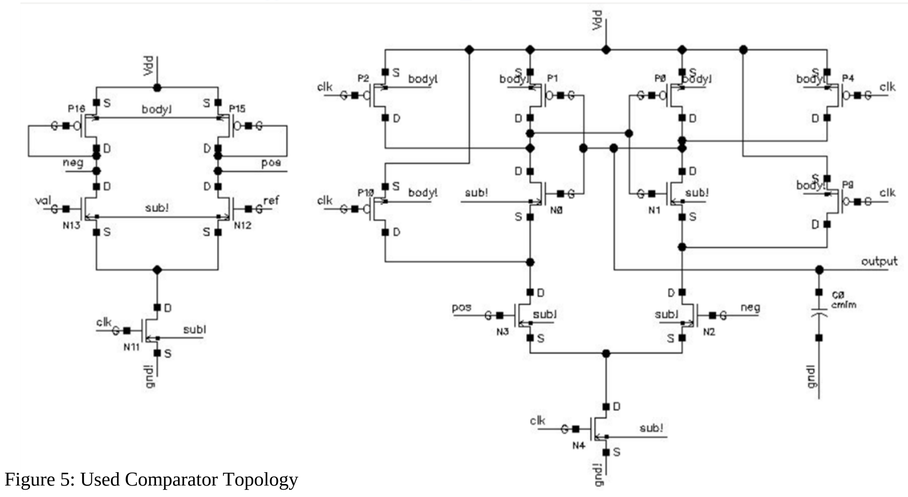

Figure 5: Used Comparator Topology

- Consists of preamplifier stage and decision stage.
- If value is higher than or equal to reference, output voltage is equal to Vdd, 1.2 Volts.
- If value is lower than reference, output voltage is 0 Volts.
- The circuit resets itself with each clock pulse, making another decision each time clock reaches 0 Volts.

Output

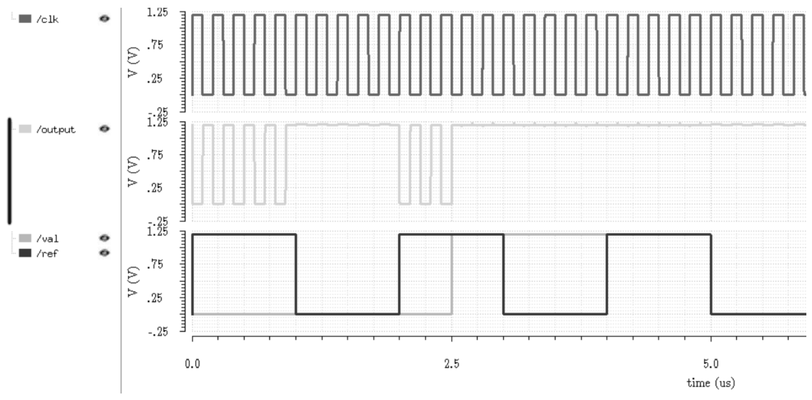

Figure 6: Comparator Simulation Results

Specifications

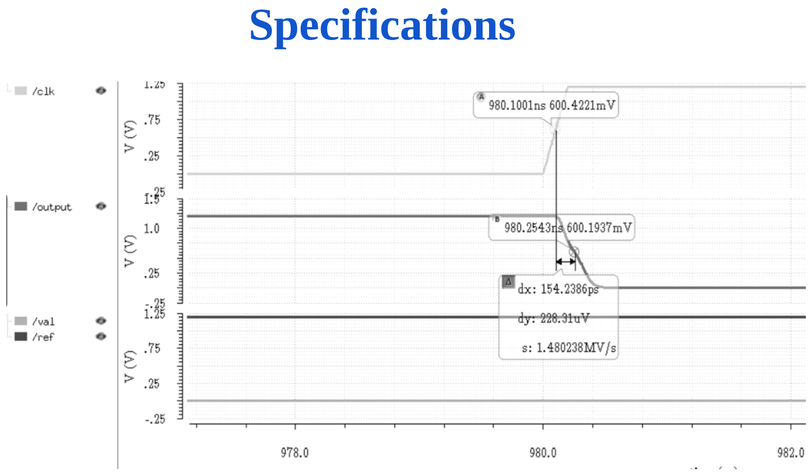

Figure 7: Logic 0 Decision Time

- Decision time for logic 0, which means the time between half of the clock voltage (600 mV) and half of the output voltage (600 mV), is measured as 154 pS.

	Proposed	Progressed at Midterm	Current Status	State of the Art in this Technology
Decision Time	300 pS	~275 pS	~150 pS	23.3 pS
Power	1 nWatt	0.27 nWatt	0.3 nWatt	Nano Watt range

Table 1: Aimed and Achieved Specifications