Transistor Level Comparator Design

İpek Gerdan
Sabancı University / EE / Sophomore
ipekgerdan@sabanciuniv.edu

Alperen Yaşar
Sabancı University / EE / Sophomore
alperenyasar@sabanciuniv.edu

Supervisors:

Yaşar Gürbüz / EE
Ömer Ceylan / EE
Melik Yazıcı / EE

Abstract

Analog to digital converters are critical components for digital world of signal processing systems as communication systems. A comparator is a sub-circuit of the analog to digital converters which is responsible of comparing two given voltage values, and give a binary logic decision. This paper studies transistor level comparator which is including its state of the art, its working mechanism. To survey the transistor level comparator topology, the sub circuit designed for usage in high speed and low power analog to digital converters. As the 130 nM technology allows, the decision time of the comparator appears 140 pico Seconds on average and a power consumption of 0.3 nano Watts.

Index Terms- Analog to digital convertor, transistor level comparator, decision time, power dissipation, preamplifier stage, decision stage.

Index

1. Introduction

Analog to digital converters (ADC) are abundantly used in many digital circuits that require an analog input from environment or preceding analog circuit. Mobile phones are a typical case for the usage of such converters. Received analog signal via antenna should first be digitalized before going into a digital microprocessor. To have a better accuracy and precision in conversion process, ADC circuits should be able to work power efficient and fast, in order to increase the sampling rate of the analog signal.

Inside the ADC, there is a sub circuit that is called comparator. These comparators typically have two inputs, and single output. It is responsible of comparing two given voltage values, and give a binary logic decision. Using this circuit over and over again, ADC will be able to map a voltage value to digital, binary sequence. At each iteration, accuracy of the digital output will be closer to analog value. Thus, comparator should be able to work in high speed in order to achieve a good conversion accuracy. In this research project, it was aimed to build a high-speed and low power comparator, using 130 nM CMOS transistor technology.

2. Analog and Digital Signals

Analog signals are waveforms that are continuous in time and value domain. These signals create problems while storing or processing in digital circuits. Storing continuous sin(x) function in a computer is a basic yet explanatory example. If a user wants to store values for sin(x) between 0 and π radians, an infinitely large storage is needed. That's because between 0 and π, there are uncountable-infinitely many numbers. To store sin(x) perfectly, for each infinitely many x input, we must store infinitely many sin(x) output.

A solution for this is to take samples from the analog signal. Instead of storing every single value for sin(x), one can decide on a sampling rate. If sampling period is set to be 0.1 radians, conversion will be made by taking 31 discrete samples from the sin(x) function. Instead, if the sampling period is set to be 0.01 radians, 314 samples will be taken from same signal. As the number of samples increases; in other words, as sampling frequency increases, resultant digital signal will look more like the original analog one.

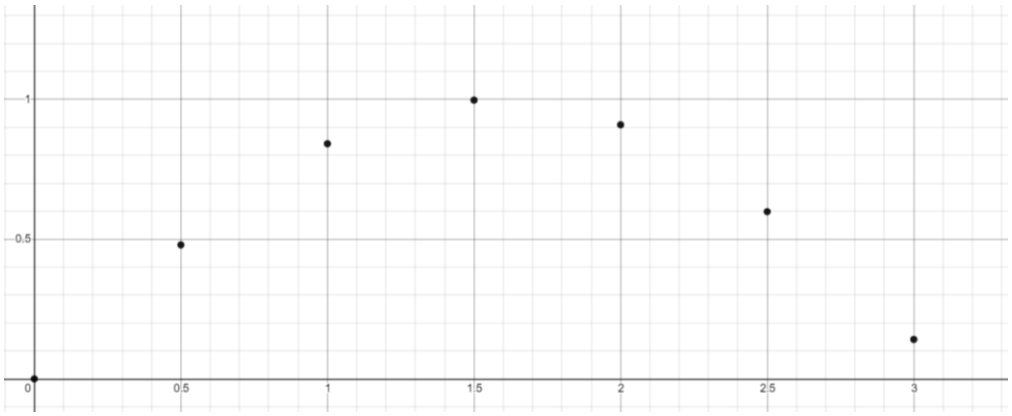

Figure 1: Sine function with 0.5 radians sampling period

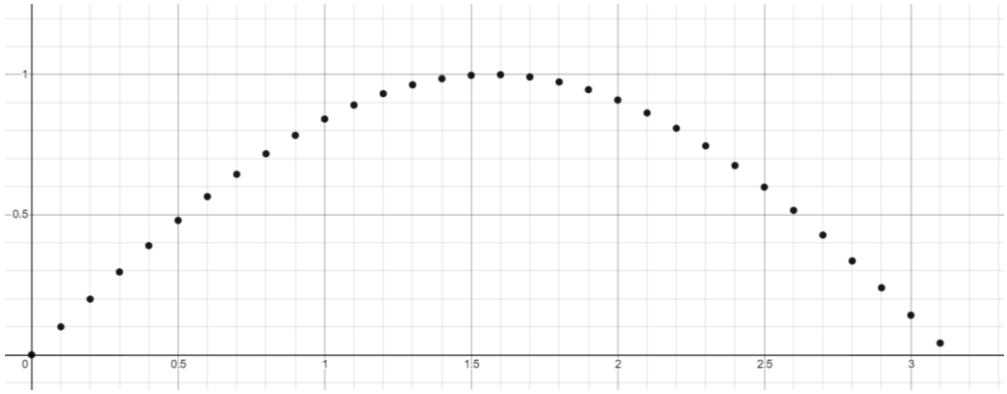

Figure 2: Sine function with 0.1 radians sampling period

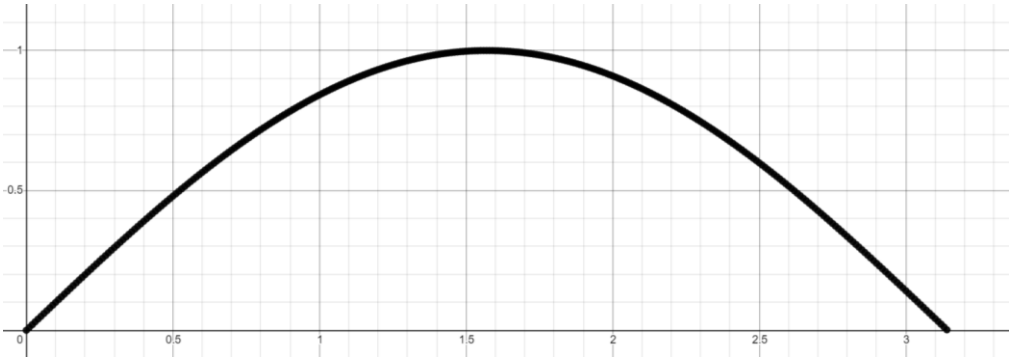

Figure 3: Sine function with 0.01 radians sampling period

According to Shannon-Nyquist theorem, sampling frequency should be at least twice of the highest frequency in the signal. For instance, if our sin(x) function has a frequency of 440 Hz (A, La note), it should be sampled with at least 880 Hz frequency. In practice, it should be much higher for better quality. That's the reason why an ADC circuit should be able to operate in very high speeds.

3. Analog to Digital Converter

Analog to digital converters are iterative circuits that try to map an analog voltage value to binary digital value. The number of bits that will represent a single voltage value is called *resolution*. If the resolution is 10, analog value will be represented with 10 bit number, which means between 0-1023 in decimal system. As the resolution increases, precision of the conversion but also number of iterations increases, creating a trade-off between accuracy and time/ power consumption.

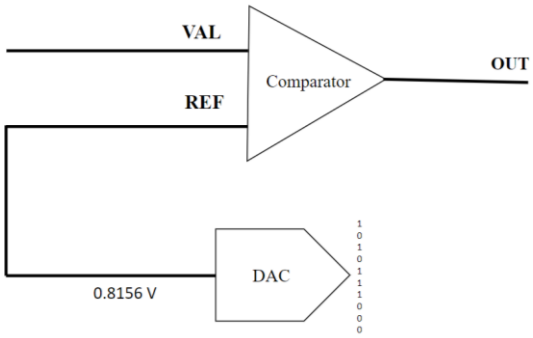

Figure 4: ADC Outline

As it can be seen in figure 4, a basic ADC outline consists of a comparator and Digital to Analog Converter (DAC). DAC will generate a voltage value between 0V and max voltage depending on the given binary input. If the max voltage value is 1.2 Volts, 1010111000 will generate 0.8156 V of voltage. Comparator will compare given signal (VAL) and reference voltage coming from DAC. If value is higher than reference, it will give an output of max voltage (1.2 Volts in this example), logic 1. DAC will increase the next bit and check if the reference value is now higher or lower than the signal value. If a resolution of 10 is used, at 10 iterations ADC will be able to convert an analog voltage to a number between 0 and 1023.

4. Design of Comparator in Transistor Level

a. Methodology

Comparator circuit was designed in Cadence Virtuoso, a software which allows to build and simulate integrated circuits. 130 nM technology was used, which determines the minimum length of the transistor. Different topologies were tested before determining on this one, which will be introduced later on in this section. Two mainly focused aspects were decision time and the power consumption of the circuit. It was aimed to reach a reasonably good speed to power consumption ratio. A literature review is made with other works in this topic, to see which topology they have used and its effects.

b. Properties of Comparators

i. Order of Comparator

Order of the voltage transfer function of the comparator determines its transition speed. Ideally, comparator works in zero order which can suddenly change state when two inputs are equal to each other.

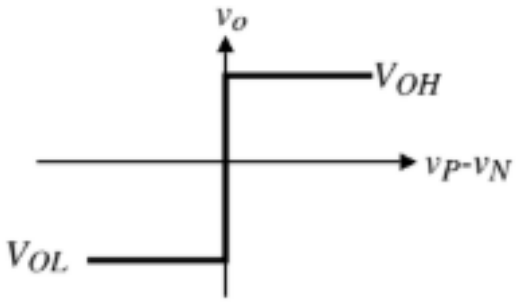

Figure 5: Zero Order Transfer Function

As it can be seen from figure 5, if the difference between positive (value) and negative (reference) inputs of the comparator is 0, state of the output suddenly changes from logic 0 to logic 1. However, as mentioned before, this is not the realistic case and comparators actually have a transfer function of first order.

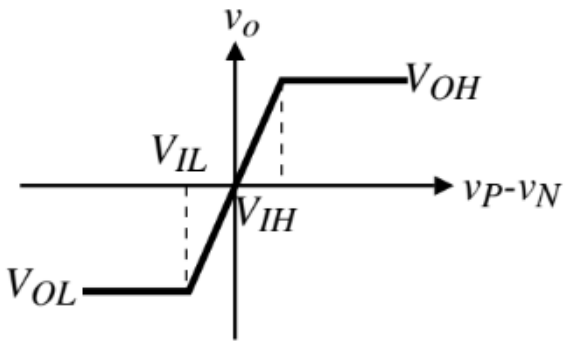

Figure 6: First Order Transfer Function

In figure 6, it can be seen that output starts climbing to logic 1 state before positive input is higher than negative input. This linear increase creates a delay in decision when difference between inputs are in that linearly increasing region. That's why it was aimed to make this transition stage as small as possible, trying to "reach" the zero order transfer function.

ii. Offset Voltage

Transfer function of the comparator might have an offset voltage, which will basically move the graph in figure 6 in horizontal axis. This will make sure that positive input is higher than the negative input with a specified voltage to return logic 1 output. This can be better understood with the graph on Figure 7. In this project, we are not aiming to have a offset voltage.

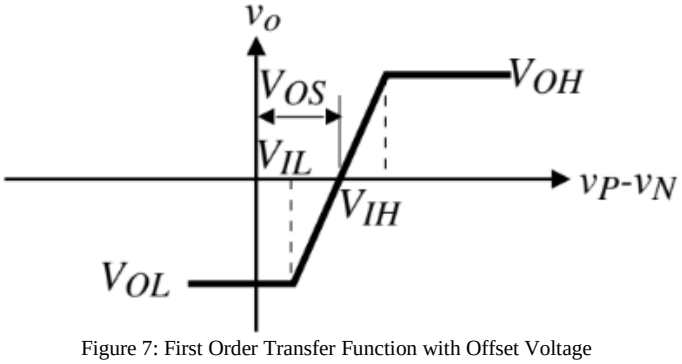

Figure 7: First Order Transfer Function with Offset Voltage

c. Topology

Designed comparator consists of two stages: preamplifier stage and decision stage. Preamplifier stage is a single stage differential amplifier circuit that has two inputs and two outputs. These outputs from preamplifier is than fed to the decision stage circuit.

i. Preamplifier Stage

This stage had two main contributions to the comparator. As mentioned before, it was aimed to create a circuit with transfer function of almost zero order. Also this stage decreases our decision time, increasing the speed of the comparator.

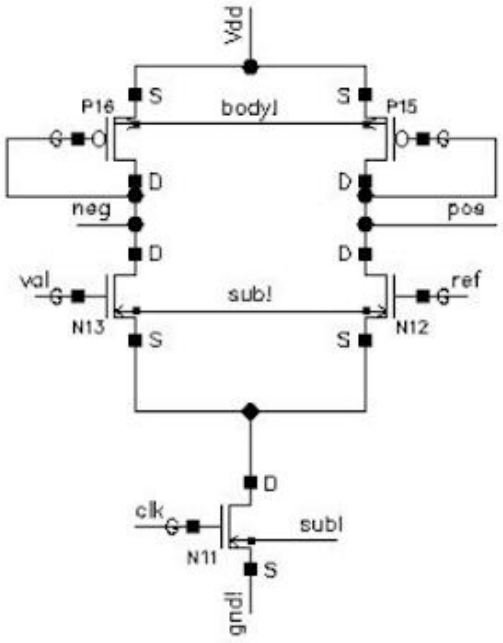

Figure 8: Preamplifier Stage

As shown in figure 8, two inputs, value and reference, is given through the gate terminals of the NMOS transistors in both ends. Outputs that are taken above the NMOS are connected into the second stage. The NMOS transistor at the bottom acts as a current source, which is connected to the

clock pulse. Clock pulse can be thought of as a square wave with very high frequency. Visualization of it will be given in the upcoming chapter.

ii. Decision Stage

This is the stage where comparator compares two given inputs and gives a decision on which one is higher. If value (pos) is higher than reference (neg) voltage at the output will be equal to Vdd, which is 1.2 Volts. Else, the output will be 0 Volts.

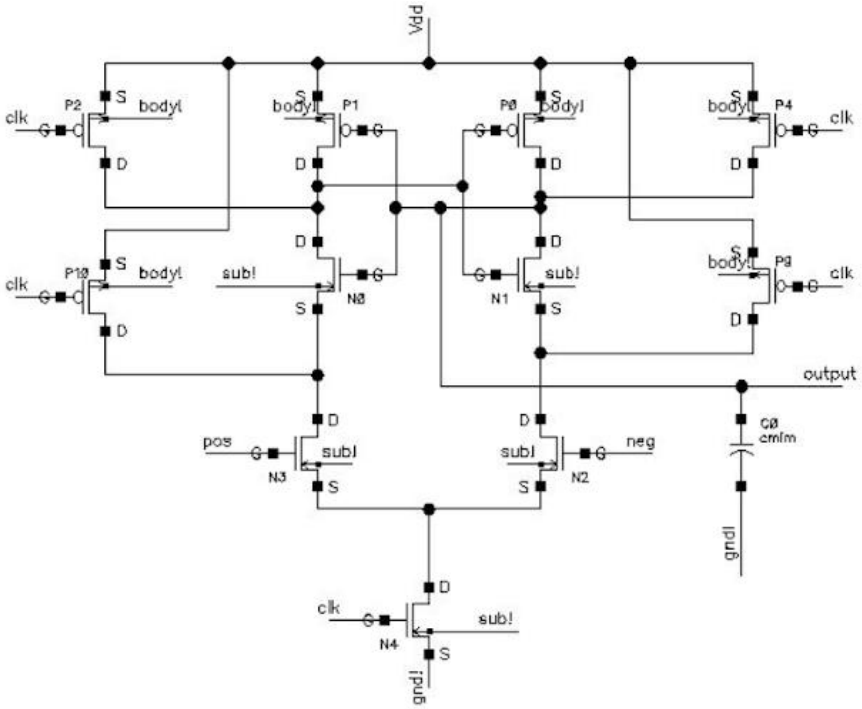

Figure 9: Decision Stage

Four PMOS transistors in far left and right sides are used to reset the whole circuit before making another decision. As they are PMOS, when clock decreases to zero, transistors start operating and reset the circuit from 4 points, connected through their drain terminals. When the clock rises to high, circuit now gives a decision and generates an output. As in the previous stage, NMOS transistor at the bottom is used as a current generator. It is again connected to clock from its gate terminal. Structure at the middle top is called latch. It is the place where decision is made and stored. 70 femto Farad capacitor is connected to the output as a capacitive load, in order to have more realistic results while simulating the circuit. Without adding it, circuit would work much faster, but it wouldn't be a realistic result, as this comparator will be preceding another circuit to be used.

5. Results and Analysis

a. General Output

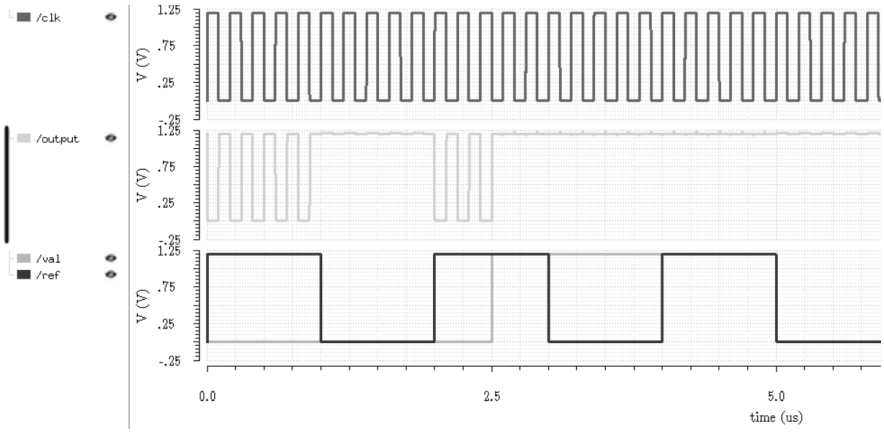

Figure 10: Transient Simulation Result

It can be seen that designed comparator works properly, giving a decision of 0 Volts when value is higher than or equal to reference voltage. Clock signal that was mentioned before can be seen in the most upper graph. Each time it rises to 1.2 Volts (Vdd), circuit gives another decision output. When it falls to 0 Volts, output becomes 1.2 Volts, following the clock. This is not the decision and must not be confused. It is due to reset state of the circuit.

b. Decision Time

In ADC circuits, thus in comparators time efficiency is very crucial. That's why it is important to check the decision time of the built circuit. As the maximum Vdd voltage is 1.2 Volts, decision time will be measured as the time delay between clock and output signal to reach 0.6 Volts.

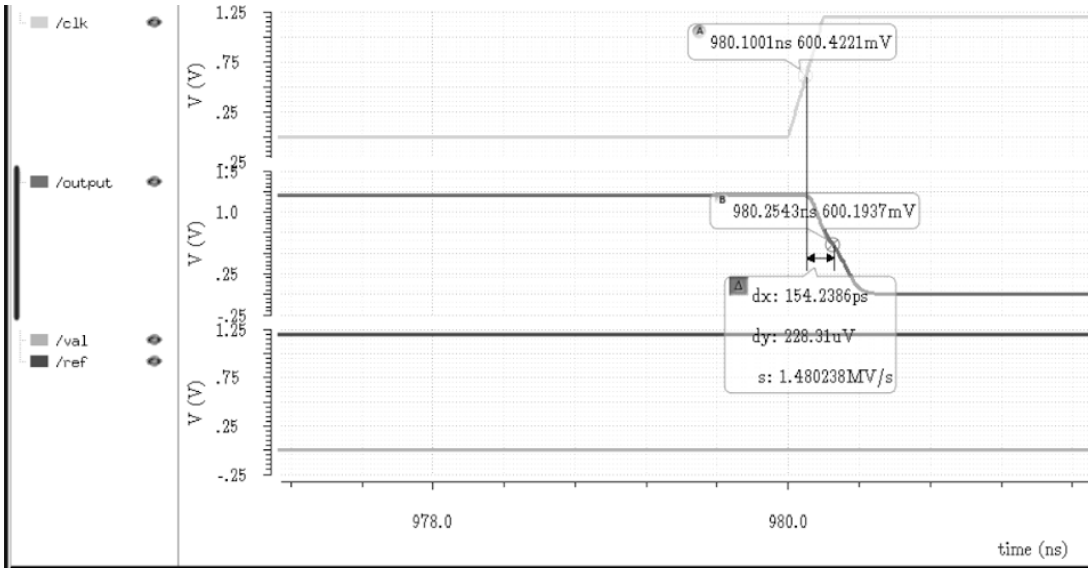

Figure 11: Decision Time Measurement

As shown in figure 11, decision point can be measured as 154 picoseconds. This means between clock and decision, there is only 154 picoseconds of delay. Decision time in figure 11 is measured for logic 0 output. When logic 1 output was measured with the same principle, it is seen that the decision time is 136 picoseconds. On average, the circuit requires around 140 picoseconds to have a decision.

c. Power Consumption

Power consumption is another crucial specification for ADC circuits. As they are being used over and over again for a very long time, they should be able to operate with low power consumption. However, because there is a tradeoff between speed and power consumption, it was aimed to find an optimal speed to power ratio. When circuit is simulated, it's seen that it has a power consumption of 0.3 nano Watts.

d. Aim, Progression and State of the Art

Before starting to design and build the comparator circuit, some specifications were determined. It was aimed to reach a maximum decision time of 300 picoseconds, and maximum power consumption of 1 nano Watt. By the middle of the development progress, 275 picoseconds and 0.27 nano Watt power consumption was achieved. In its current status, the circuit reached a decision time of 140 pico Seconds on average and a power consumption of 0.3 nano Watts. Power consumption increased from its last state. However, when speed to power ratio is considered, current status is almost twice good than the previous state. During literature review, the fastest comparator using 130 nano Meter technology we had found had a decision time of 23.3 pico Seconds and a power consumption at nano Watt range (was not specified). When compared to state of the art, the circuit built in this project should be developed further more to increase the speed. However, the specific power consumption of the state of the art is not known, increasing the speed with a tradeoff in power might be considered, still holding the consumption in nano Watt range.

	Proposed	**Progressed at Midterm**	**Current Status**	**State of the Art in this Technology**

Decision Time	300 pS	~275 pS	~150 pS	23.3 pS
Power	1 nWatt	0.27 nWatt	0.3 nWatt	Nano Watt range

Table 1: Aimed and Achieved Specifications

6. Conclusion

In this project, it was aimed to design a comparator with 130 nM transistors, for usage in high speed and low power analog to digital converters. The topology of the comparator within its 130 nM technology allowes the decision time of the comparator 140 pico Seconds on average and a power consumption of 0.3 nano Watts. Even though specifications that were determined before designing the circuit are satisfied and actually doubled, this design is open for new developments in order to reach the speed of state of the art in this technology.

7. References

- A New Ultra Low Power High Speed Dynamic Comparator, Khalafi, Ali, Ahmad Rabiei, Arman Najafizadeh, 2015
- HIGH-SPEED AND LOW-POWER DYNAMIC LATCH COMPARATOR, Moni, Jackuline, P. Jisha
- Allen, P. E., & Holberg, D. R. (2016). *CMOS analog circuit design*. New Delhi, India: Oxford University Press.